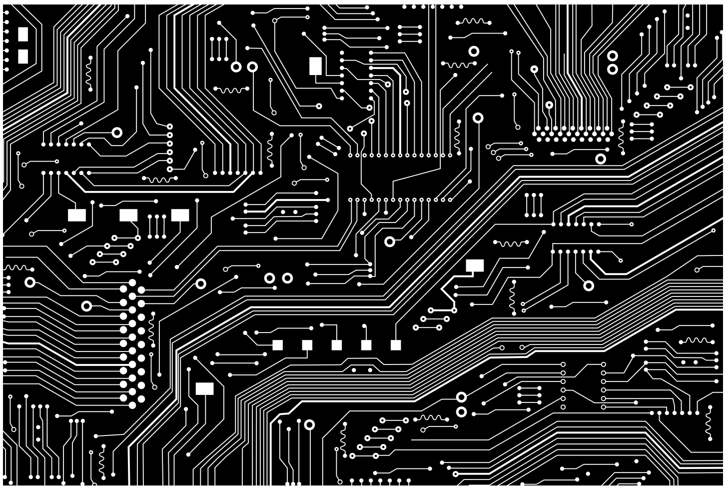
INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

A Nanoscale Si-Based Two-Terminal Reconfigurable Switch

TECHNOLOGY NUMBER: 4182



OVERVIEW

Nanoscale resistive switches using a-Si for high-density memory applications

- Enables controlled, high-precision memory switching at nanoscale with high throughput
- High-density memory storage, reconfigurable interconnects, and advanced logic circuits

BACKGROUND

The semiconductor industry's trend toward miniaturization necessitates new device concepts and architectures to sustain scaling. Traditional transistors are nearing their physical limits, prompting interest in two-terminal hysteretic resistive switches, known as memristors. Memristors have shown promise for ultra high-density memory storage and reconfigurable logic due to their small cell size, large connectivity, and defect tolerance. Conventional resistive switching devices use binary oxides and ionic conductors, relying on conductive filament formation through Joule heating and electrochemical processes. However, these devices face challenges like inconsistent filament formation and high-power consumption. An improved resistive switching method that offers precise control over filament formation and operates efficiently at nanoscale dimensions is essential for advancing memory and logic technologies.

INNOVATION

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Category
Hardware
Engineering & Physical Sciences
Semiconductor, MEMS, and Electronics

Inventor
Kuk-Hwan Kim
Sung Hyun Jo
Wei Lu

Further information
Joohee Kim
jooheek@umich.edu

View online

Researchers at the University of Michigan have developed a nanoscale resistive switch based on an a-Si pillar structure, offering precise control over filament formation. This device consists of a nanoscale a-Si pillar between top Ag and bottom p-Si electrodes, embedded in an insulating dielectric like cured spin-on-glass (SOG). The new design ensures high yield and uniformity, with performance metrics such as <50 ns programming time, ON/OFF ratios of 10^4-10^7, and endurance over 10^5 cycles. The nanoscale switch operates by forming and retrieving Ag filaments through programmable voltage pulses, enabling both digital and analog switching. This technology is compatible with CMOS structures and allows multilayered 3D integration. Potential applications include ultrahigh-density memory storage, reconfigurable interconnects, and advanced logic circuits in hybrid nano/CMOS architectures, providing a scalable, efficient solution for future electronic devices.

ADDITIONAL INFORMATION

REFERENCES:

Jo, Sung Hyun and Kim, Kuk-Hwan and Lu, Wei, " Programmable Resistance Switching in Nanoscale Two-Terminal Devices," Nano Letters, Year 2009, Volume 9, Number 1, Pages 496--, doi: 10.1021/nl803669s

INTELLECTUAL PROPERTY:

US8687402 “Silicon-based nanoscale resistive device with adjustable resistance”