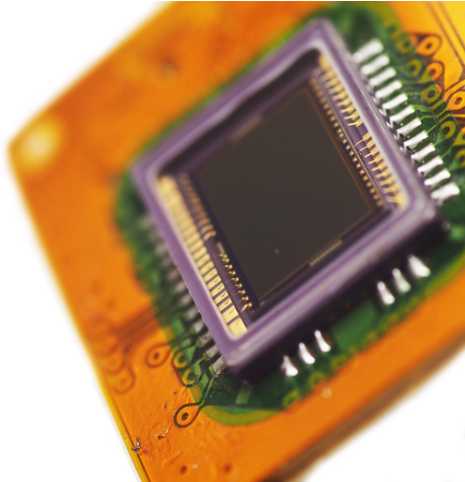




# A Photodetector Based on Double Layer Heterostructures

Technology Number: 5456



Technology ID

5456

## Category

Hardware

Engineering & Physical Sciences

Semiconductor, MEMS, and

Electronics

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## OVERVIEW

Low-cost, high-responsivity, CMOS-compatible photodetector architecture

- Enhances integration, reduces cost, and supports broad-spectrum detection
- Ideal for photodetectors, image sensing, and on-chip integration

## BACKGROUND

Photodetectors play a critical role in imaging and sensing technologies, requiring high responsivity and broad-spectrum detection capabilities. Traditional high-responsivity photodetectors, such as avalanche photodetectors and photomultipliers, are effective but suffer from significant drawbacks, including bulkiness and the need for high external bias voltages. These factors hinder their integration with silicon-based technologies and the development of on-chip imaging arrays. Phototransistors present a potential alternative, but their high-cost epitaxial growth processes and low operating temperatures limit widespread practical applications. There is a necessity for a cost-effective, high-performance photodetector that is compatible with CMOS manufacturing processes, enabling seamless integration into existing silicon-based systems and fostering advancements in imaging and sensing applications.

## INNOVATION

Researchers at the University of Michigan have developed a novel photodetector architecture that addresses the limitations of existing technologies. The design features two closely spaced light-absorbing material layers separated by a thin-film insulator, which effectively isolates the layers electrically without light excitation and voltage bias. When optically excited, photoexcited electron-hole pairs are generated, and with back-gate biasing, the insulator functions as a hole-blocking layer facilitating electron tunneling to the bottom layer. This architecture supports high responsivity, broad-spectrum detection, and a simple planar structure with a compact footprint. Crucially, it is CMOS-compatible and low-cost, eliminating the need for high-cost doping or epitaxial growth. Applications include photodetectors, image sensing, and on-chip integration, enabling significant advancements in these fields.

## **ADDITIONAL INFORMATION**

[US9680038](#) "Photodetectors based on double layer heterostructures"