INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

A Relaxation Oscillator-Based Probabilistic Combinatorial Optimization Engine for Soft Decoding of LDPC Codes

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Hardware
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OVERVIEW

Oscillator-based computation engine for efficient, robust soft decoding of LDPC error-correction codes

- Achieves faster, lower-energy, and more robust soft LDPC decoding using quantum-inspired, massively parallel analog computation
- Wireless communications, data storage, 6G/5G, satellite links, error-resilient IoT, high-speed networking hardware

BACKGROUND

Error-correcting codes, including Low-Density Parity-Check (LDPC) codes, are fundamental for reliable data transmission and storage in modern communications systems. Traditionally, LDPC decoding relies on belief propagation (BP) or related digital algorithms executed on sequential processors or dedicated ASICs. While such approaches are well-established, they face increasing limitations in energy efficiency, throughput, and scalability, especially as system complexity grows with higher data rates and denser code structures. Quantum annealers, and analog and oscillator-based systems, have shown promise for certain combinatorial optimization problems but historically suffer from limited connectivity, coarse initializations, high power consumption, or unsuitable architectures for soft decoding. To meet the demands of next-generation

communications and low-power edge or IoT systems, there is a need for energy-efficient, scalable, and robust decoding engines that directly map problem structure and leverage parallel continuous-time dynamics for improved error correction.

INNOVATION

Researchers at the University of Michigan have developed the first oscillator-based combinatorial optimization engine enabling robust, high-throughput, one-shot soft decoding of LDPC codes. Leveraging continuous-time analog computation inspired by quantum systems, the engine uses 28nm CMOS relaxation oscillators (RXOs) with digitally controlled, multi-body (k=6) coupling matched to LDPC Tanner graphs. Unlike prior quantum or analog decoders that require iterative or energy-intensive computing, this architecture directly encodes soft input data as initial oscillator phases and achieves solution convergence in a single operation cycle. The core includes precise, digitally-configurable phase initialization, robust feedback via digital crossbars, and in-oscillator DACs, enabling robustness to noise, voltage, and temperature. Prototyped with 96 oscillators, it achieves leading error and power performance: Frame/Bit Error Rates of 1.38 x 10^-5 / 1.25 x 10^-6 at 7dB SNR and 5.26pJ/bit, far surpassing recent digital and analog state-of-the-art. It is highly adaptable for other optimization tasks (e.g., Max-Cut, k-SAT) spanning advanced communications, sensing, and cryptography.

ADDITIONAL INFORMATION

REFERENCES:

- "A Relaxation Oscillator-Based Probabilistic Combinatorial Optimization Engine for Soft Decoding of LDPC Codes"

INTELLECTUAL PROPERTY:

Patent application pending.

KEYWORDS:

Oscillator-based Computing, Combinatorial Optimization, Quantum-inspired, Hardware Accelerator