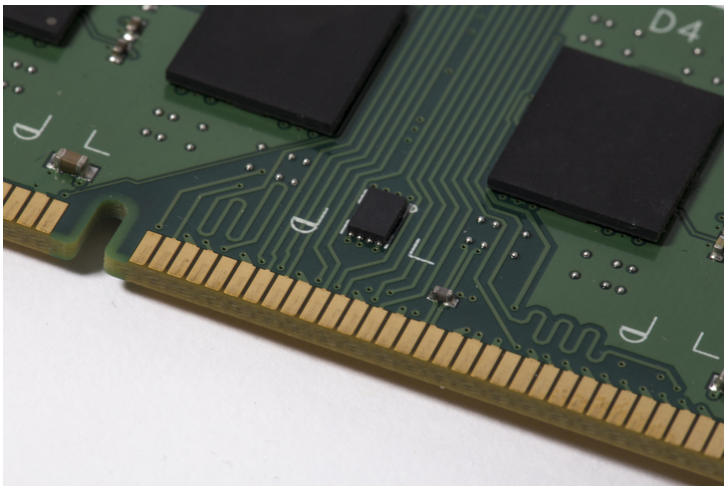
INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

Drift Tolerant Read/Write Scheme for Multi-Bit Resistive RAM

TECHNOLOGY NUMBER: 6784



Technology ID
6784

Category
Hardware
Engineering & Physical Sciences
Semiconductor, MEMS, and Electronics

Inventor
Pinaki Mazumder
Yalcin Yilmaz

Further information
Joohee Kim
jooheek@umich.edu

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OVERVIEW

A novel memory scheme for stable multi-bit memristor storage

- Improved read/write stability with reduced feedback complexity
- ReRAM, Nonvolatile memory, solid-state drives, cloud storage solutions

BACKGROUND

Over the years, the demand for high-density, reliable, and scalable memory technologies has exponentially increased, particularly with the proliferation of portable electronics and cloud computing. Traditionally, Flash memory filled this need but is now reaching physical scaling limits. Flash memory faces reliability challenges like charge leakage and capacitive coupling, reducing performance integrity. As a result, alternative nonvolatile memories have been explored—namely, memristor-based memories, known for their high density, scalability, and endurance. Initial approaches with memristors incorporated complex peripheral circuitry to address feedback and resistance variability, which introduced unwanted latency and increased fabrication costs. These limitations underscore the need for a simpler yet efficient memory management approach that seamlessly integrates with existing CMOS technology.

INNOVATION

Researchers at the University of Michigan have developed a drift-tolerant read/write scheme for a memristor-based multilevel memory that addresses scalability and reliability concerns. It introduces reduced-constraint monitoring to achieve multibit per cell storage with significantly lower hardware complexity, minimizing latency and supporting CMOS-compatible voltages. The method ensures dependable state differentiation despite potential resistance drift—lessening refresh frequency requirements. Real-world applications include high-density nonvolatile memories like solid-state drives, enhancing data retention for enterprise storage and enabling more affordable consumer electronics by reducing manufacturing costs. This architecture supports advancements in nanotechnology-based logic circuits and can be applied to data-intensive fields such as neural computing and image processing, fostering future developments in memory-centric technologies.

ADDITIONAL INFORMATION

REFERENCES

Y. Yilmaz and P. Mazumder, "A Drift-Tolerant Read/Write Scheme for Multilevel Memristor Memory," in IEEE Transactions on Nanotechnology, vol. 16, no. 6, pp. 1016-1027, Nov. 2017, doi: 10.1109/TNANO.2017.2741504

INTELLECTUAL PROPERTY

US9941003 "Multi-level resistive memory structure"