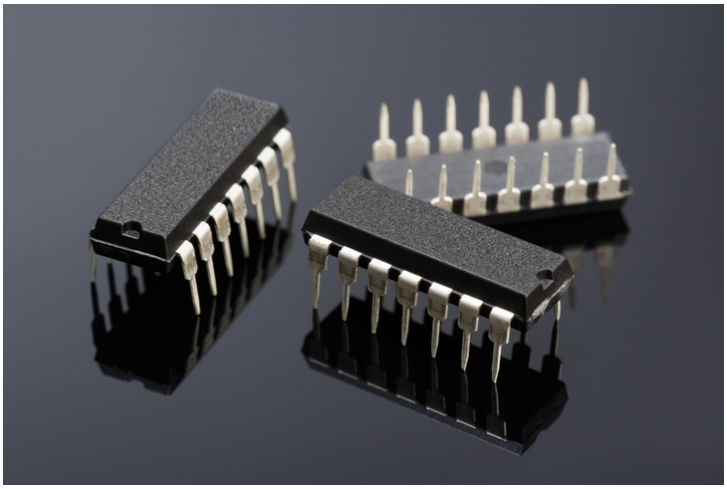
INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

Low-Power Area-Efficient SAR ADC

TECHNOLOGY NUMBER: 4494



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Category
Hardware
Engineering & Physical Sciences
Semiconductor, MEMS, and Electronics

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OVERVIEW

Area-efficient, low-power 8-bit SAR ADC with dual capacitor arrays for neural interfaces

- Reduces space by 80% and power consumption by 85%
- Applications in simultaneous, real-time multi-site neural monitoring

BACKGROUND

Monitoring neural activity in real-time is crucial for understanding neural functions and developing neuroprosthetics. Historically, neural activity monitoring involved single or limited-site recordings with wire-based or bulky electronics, leading to spatial constraints and introducing noise. Existing technologies often suffer from high power consumption and large form factor due to capacitor arrays in analog-to-digital converters (ADCs). Modern advancements include multi-channel neural interface systems which require efficient, low-power, compact ADCs for simultaneous data acquisition from multiple neural sites. As resolution increases, the space and power consumed by these capacitor arrays become significant limitations, necessitating a more efficient method. There is a critical need for ADCs that minimize area and power consumption while enhancing performance and reliability in neural monitoring.

INNOVATION

University of Michigan researchers have developed a 8-bit SAR ADC utilizing dual capacitor arrays, significantly improving area and power efficiency. This design reduces the required capacitor array area by 80% and cuts power consumption by 85% compared to conventional ADCs. By employing dual capacitor array banks, the new ADC achieves a compact form factor and eliminates power loss from charging and discharging processes without leakage. These technical advances allow the implementation of multiple ADCs within the same space, facilitating more comprehensive and simultaneous neural activity monitoring. Potential real-world applications include advanced neural interface systems for brain-computer interfaces, neuroprosthetics, and extensive neuroscientific research, providing a more refined and efficient toolset for real-time neural data acquisition and analysis.

ADDITIONAL INFORMATION

REFERENCES:

S. -I. Chang and E. Yoon, "A low-power area-efficient 8 bit SAR ADC using dual capacitor arrays for neural microsystems," 2009 Annual International Conference of the IEEE Engineering in Medicine and Biology Society, Minneapolis, MN, USA, 2009, pp. 1647-1650, doi: 10.1109/IEMBS.2009.5333068

INTELLECTUAL PROPERTY:

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