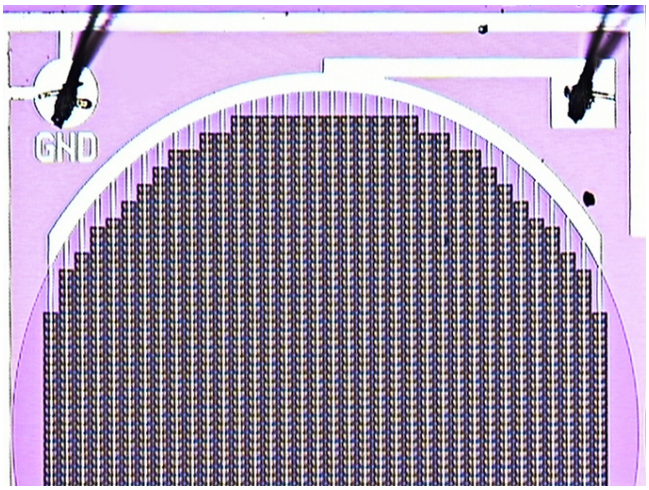
INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

Low-Power, Low-Noise Open-Loop CMOS Preamplifier

TECHNOLOGY NUMBER: 4194



OVERVIEW

Energy-efficient pseudo open-loop amplifier for neural interface systems

- Provides low power consumption and noise efficiency for long-term neural monitoring
- Neural data acquisition, brain-computer interfaces, and medical diagnostics

BACKGROUND

Advances in CMOS technology have enabled significant progress in developing multichannel implantable neural systems. However, long-term monitoring of brain activity remains challenging due to stringent hardware constraints, including power consumption, noise levels, and area limitations. Traditional front-end preamplifiers using closed-loop topologies with input transistors offer reliable performance but suffer from stability constraints that limit power-noise efficiency. Alternative low-power open-loop amplifiers have been explored, but their single-ended output is susceptible to common-mode noise and supply fluctuations. These shortcomings create a need for more efficient and reliable amplifiers capable of maintaining high linearity and stable operation across various conditions, particularly for applications requiring continuous monitoring of neural signals. An improved method is essential for advancing neural interface technology, enabling more accurate and energy-efficient data acquisition in medical and research contexts.

Technology ID

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Category

Hardware
Engineering & Physical Sciences
Semiconductor, MEMS, and Electronics

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INNOVATION

University of Michigan researchers have developed an energy-efficient pseudo open-loop amplifier with a programmable band-pass filter designed for neural interface systems. The amplifier operates with a power consumption of 400nA at a 2.5V power supply, achieving a thermal noise level of 85nV/Hz and an input-referred noise of 1.69 microVrms from 0.3Hz to 1kHz. This innovation presents a noise efficiency factor of 2.43, which is the lowest reported for differential topologies to date. The bandwidth of the preamplifier can be controlled from 138mHz to 2.2kHz by programming the switched-capacitor frequency and bias current, allowing it to meet various application requirements. The compact design, realized in an area of 0.043mm^2 using 0.25m CMOS technology, offers high linearity and stable operation over process and bias variations. Potential real-world applications include neural data acquisition, brain-computer interfaces, and medical diagnostics.

ADDITIONAL INFORMATION

REFERENCES:

S. -I. Chang, S. -Y. Park and E. Yoon, "Low-Power Low-Noise Pseudo-Open-Loop Preamplifier for Neural Interfaces," in IEEE Sensors Journal, vol. 17, no. 15, pp. 4843-4852, 1 Aug.1, 2017, doi: 10.1109/JSEN.2017.2717787

INTELLECTUAL PROPERTY:

US8922274 “Bioamplifier for neural interfaces"