INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

Parallel Non-Volatile Memory (NVM) Crossbar Array Switch Interface Module

TECHNOLOGY NUMBER: 2020-472

OVERVIEW

A new means for optimizing crossbar array non-volatile memory (NVM) technologies

- Mixed-signal circuits for high-voltage for WRITE operations and low-voltage for READ operations
- A fast, low-cost, and high-density architecture for non-volatile memory

BACKGROUND

Crossbar array non-volatile memory (NVM) technologies are used for high-density memory applications and consist of horizontal and vertical wires that intersect at specific points. Memory elements at these points can be programmed to exist in either a high or low resistance state, representing a binary one or zero. The analog and digital circuit hardware that functions on the non-volatile memory crossbar arrays connects to the periphery of the crossbar structure through an analog switch matrix. While row hardware is designed to match the pitch of the NVM crossbar array rows, column hardware matches the pitch of the NVM crossbar array columns. Specialized mixed-signal circuits provide high-voltage to write NVM devices versus low-voltage to read programmed NVM devices. In spite of the advantages of this arrangement, a need exists for improved efficiency of NVM technologies.

INNOVATION

Researchers have created a technology that consists of row hardware and column hardware which provide the minimum number of switches and high-voltage level shifters for mixed high voltage and low voltage operation of computer circuits. This technology is a unique architecture for both the row and column switch matrix that is connected to a crossbar array non-volatile memory. It includes mixed-signal circuits that provide high-voltage for WRITE operations and low-voltage for READ operations of the non-volatile memory. This approach therefore provides a fast, low-cost, and high-density architecture for non-volatile memory. Its high-density is particularly advantageous for applications that require low physical footprints. Overall, this innovation creates efficiencies in the hardware component of these crossbar array non-volatile memory technologies by reducing the number of components required to implement mixed high-voltage and low-voltage operation.

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Category

Hardware

Engineering & Physical Sciences

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