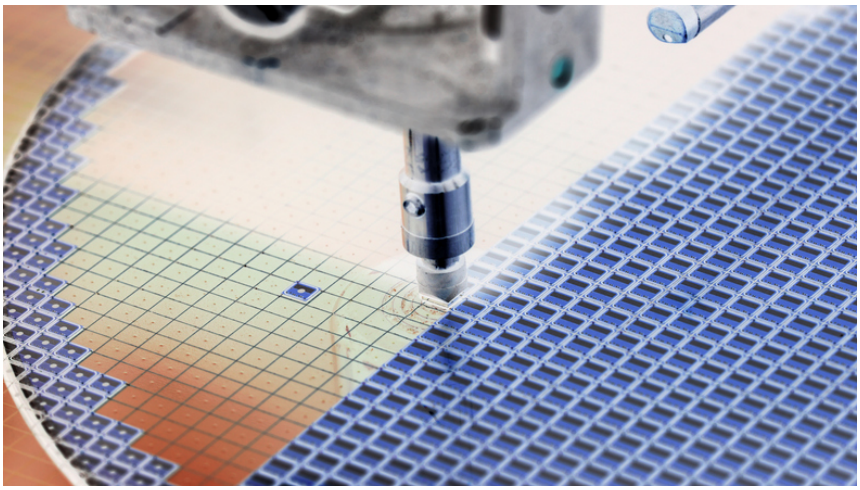
INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

Robust 13T SRAM Cell for Improving Write Margin in Ultra-low Power Applications

TECHNOLOGY NUMBER: 5937



OVERVIEW

Enhanced 13T SRAM bitcell design for improved write margin and reliability

- Eliminates charge contention, increasing write margin
- Ultra-low power applications, reliable digital CMOS systems, SRAM-based designs

BACKGROUND

With advancements in integrated circuit technology, process, voltage, and temperature (PVT) variations have become significant challenges, particularly impacting digital CMOS systems. Traditional CMOS circuits like SRAM cells, latches, and inverters experience reliability issues due to these variations, often leading to failure in memory operations and synchronization errors. Existing techniques to address these challenges include parallel computation, clock gating, low swing signaling, dynamic voltage and frequency scaling, and sub-threshold operation. However, sub-threshold operation, although effective at reducing dynamic power consumption, increases noise susceptibility in sequential logic, making SRAM cells particularly vulnerable. Previous SRAM designs have attempted to improve robustness against these variations by decoupling read ports, minimizing leakage, and boosting wordline voltage. Despite these efforts, improving write margin remains a complex issue due to inherent charge contention in traditional SRAM structures, necessitating a more efficient solution.

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Category

Manufacturing Process
Engineering & Physical Sciences
Semiconductor, MEMS, and Electronics

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INNOVATION

Researchers at the University of Michigan have developed 13T SRAM bitcell design to eliminating charge contention during write operations, substantially improving write margin without additional sizing constraints. This is achieved by blocking the power supply route during write operations, allowing for static operation and removing the feedback loop contention inherent in conventional SRAM cells. The design builds on a previously introduced 16T SRAM cell but optimizes it for synchronous systems by adopting a single-ended output and a simplified footer structure, reducing area and power overhead. This innovative bitcell demonstrates superior write stability and reliability, meeting stringent performance requirements for ultra-low power applications.

ADDITIONAL INFORMATION

US9627042 "Static random access memory cell having improved write margin for use in ultra-low power application"