Sub-Sampling Phase Locked Loop (SSPLL) with Saturated Reference Feedback

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OVERVIEW

Low noise, fast locking sub-sampling phase-locked loop (SSPLL) with adaptive feedback

- Uses multiplexing buffer and adaptive pulse control for improved performance
- High-frequency communications, radar systems, signal processing

BACKGROUND

Phase-locked loops (PLLs) are crucial in applications requiring precise frequency control and synchronization, such as communications and sensing systems. Traditional PLLs suffer from noise limitations due to phase detector and charge pump (PD/CP) noise, which is exacerbated in high multiplication ratios. Sub-sampling PLLs (SSPLLs) are known to address this issue by reducing PD/CP noise, particularly beneficial for high-frequency applications. However, these systems often require an additional frequency-locked loop to achieve frequency lock and can suffer from alignment issues due to process variation, temperature, and voltage (PVT) changes. These shortcomings highlight the need for faster locking times, improved noise performance, and simplified architectures without multiple loops.

INNOVATION

Researchers at the University of Michigan have developed a fast and low noise SSPLL design incorporating a multiplexing buffer and an adaptive charge pump pulse control circuit, enabling precise control over phase detection and enhanced locking performance. The multiplexing buffer allows one VCO edge per reference cycle, merging aspects of bang-bang and sub-sampling phase detection. An adaptive charge pump pulse control mechanism accelerates initial lock times and minimizes noise in the locked state. Automatic calibration accounts for PVT variations, improving alignment accuracy. This method eliminates the necessity for a secondary frequency-locked loop, simplifying the design and reducing overall power consumption. Real-world applications for this innovation span high-frequency communications, radar systems, and advanced signal processing, where reduced noise and fast locking times are critical.

ADDITIONAL INFORMATION

INTELLECTUAL PROPERTY

US 18/355,146 "Sub-Sampling Phase Locked Loop (SSPLL) with Saturated Reference Feedback"

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Category
Hardware
Engineering & Physical Sciences

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