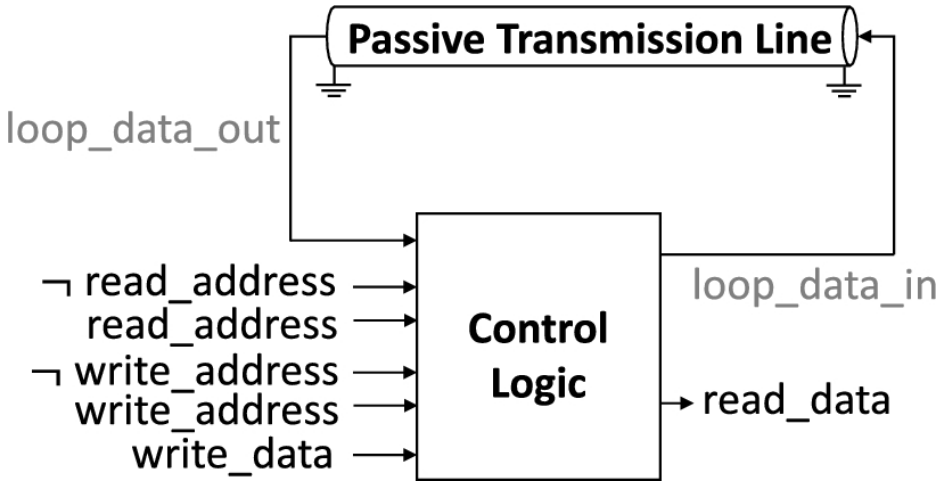
INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

# Superconductor Memory Architecture From Delay Lines

**TECHNOLOGY NUMBER: 2025-110**




## OVERVIEW

High-density, scalable superconducting memory using circulating passive transmission line delay loops

- Achieves two to three orders higher data density with minimal control circuitry and lower complexity
- Quantum-classical computers, energy-efficient data centers, cryogenic memories, security and sensing systems

## BACKGROUND

Superconductor electronics (SCEs) offer unrivaled speed, ultra-low power operation, and compatibility with cryogenic environments, marking them as ideal candidates for next-generation high-performance and quantum computing. Despite advances in logic, fabrication, and hybrid integration schemes, scalable superconducting memory remains a bottleneck. Early approaches, like single flux quantum cell arrays, were limited by transformer-based designs that hindered further density scaling, while more recent hybrid SCE-CMOS systems suffer from high latency and thermal management challenges. Explorations into new material stacks and nanowire cells have improved density, but result in complex devices or suboptimal operational characteristics when scaled. Existing superconducting memories struggle to deliver simultaneously on density, access speed, and energy efficiency. As demands for practical, high-performance SCEs grow, particularly for quantum control and data center applications, an

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innovative approach that overcomes the miniaturization and control complexity barriers is urgently needed.

## INNOVATION

Researchers at the University of Michigan have developed a fundamentally different memory architecture for superconducting systems, using passive transmission line or long Josephson junction delay loops as the storage medium. By circulating data bits within superconducting delay lines—taking advantage of their virtually zero attenuation and dispersion—this design bypasses the density limits and addressing complexity of traditional memory arrays. Data is written, read, and retained as single flux quantum pulses in circulating loops, with the architecture supporting both sequential-access and content-addressable memory modes without the need for splitters or complex control circuits. Experimental prototypes confirm operational speeds between 20–100 GHz and projected data densities in the hundreds of Mbit/cm$^2$—up to 1,000x higher than existing superconducting memory cell arrays. This advance is poised to transform memory for energy-efficient supercomputing, quantum processor control, high-security storage, and advanced cryogenic sensor platforms.

## ADDITIONAL INFORMATION

**REFERENCES:**

Volk, J., Wynn, A., Golden, E. et al. Addressable superconductor integrated circuit memory from delay lines. Sci Rep 13, 16639 (2023). https://doi.org/10.1038/s41598-023-43205-8

**INTELLECTUAL PROPERTY:**

Pending

**KEYWORDS:**

Superconducting, Memory, Quantum Computing