INNOVATION PARTNERSHIPS
UNIVERSITY OF MICHIGAN

Synthesis of Resource-Efficient Superconducting Circuits with Clock-Free Alternating Logic

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OVERVIEW

Automated synthesis of superconducting circuits using clock-free, dual-rail alternating logic.

- Eliminates clocking overhead and dramatically reduces Josephson junction count via clock-free logic synthesis
- Quantum computing interfaces, energy-efficient processors, high-speed sensing, and superconducting data centers

BACKGROUND

Superconducting electronics (SCE) promise dramatic gains in speed and energy efficiency, making them critical candidates for the next wave of classical and quantum computing and ultra-sensitive sensors. However, existing superconducting logic—particularly Single Flux Quantum (SFQ) circuits—relies on clocked gate operation, mirroring CMOS methodologies. This leads to severe overhead: up to 70% of Josephson junctions are devoted to clock management, and complex clocking limits scalability, speed, and design automation. Previous approaches to alleviating this overhead involved custom clock synchronization schemes or tool modifications, but these either increase resource costs or complicate synthesis. As a result, synthesizing arbitrary, resource-efficient superconducting circuits for practical use remains an unsolved challenge. The field requires a fundamentally new approach—one that removes the dependence on global or architectural clocks while leveraging standard automation toolchains

and established logic optimization techniques.

INNOVATION

Researchers at the University of Michigan have developed the first framework for synthesizing superconducting circuits entirely from clock-free, dual-rail alternating logic gates using the xSFQ family. By eliminating explicit clock requirements from gate semantics and employing dual-rail encoding, the approach avoids time-consuming and area-intensive clock routing, balancing, and synchronization. The invention optimizes resource usage by minimizing logic duplication and Josephson junction (JJ) count through advanced logic graph optimizations and novel storage primitives. Notably, the framework integrates seamlessly with open-source synthesis tools—enabling direct translation and optimization of both combinational and sequential designs without modifications or ad hoc workarounds. Benchmark results demonstrate an average JJ count reduction exceeding 80% compared to conventional clocked SFQ circuits. These advances unlock practical routes to efficient superconducting FPGAs, CPUs, quantum co-processors, and low-power high-rate sensor and communication systems.

ADDITIONAL INFORMATION

REFERENCES:

"Synthesis of Resource-Efficient Superconducting Circuits with Clock-Free Alternating Logic"

INTELLECTUAL PROPERTY:

Patent application pending.

KEYWORDS:

Superconducting Circuits, Clock-free Logic, Quantum Computing